AMENDMENTS TO THE CLAIMS

1. (Currently Amended): A data output circuit which outputs data on ~~an~~ internal bus lines onto ~~an~~ external bus lines, comprising:

comparison means for comparing data on groups of the external bus lines and data ~~to be output~~ on corresponding groups of the internal bus lines;

inversion means for outputting ~~a signal~~ inverted data obtained by inverting the data on ~~the~~ a respective group of internal bus lines when the number of changed bits exceeds half the total number of bits in that group on the basis of an output result from said comparison means; and

control means for outputting an inversion display signal representing that the data in a particular group has been inverted.

2. (Original): A circuit according to claim 1, wherein said comparison means, said inversion means, and said control means constitute an output data control unit.

3. (Original): A circuit according to claim 2, further comprising:

an amplifier which amplifies read data;

data latch means for latching data output from said amplifier; and

input/output means for transmitting an output data bus signal from said output data control unit as output data onto the external data bus.

4. (Original): A circuit according to claim 3, wherein said input/output means feeds back the output data to said comparison means.

5. (Original): A circuit according to claim 3, further comprising clock signal supply means for supplying a clock signal to said data latch means, said output data control unit, and said input/output means.

6. (Currently Amended): A circuit according to claim 1, wherein the data on the internal bus ~~line~~ lines includes data read out from storage means.

7. (canceled)

8. (Currently Amended): A data output method of outputting data on ~~an~~ internal bus lines onto ~~an~~ external bus lines, comprising the steps of:

arranging each of the internal and external bus lines into a plurality of corresponding groups,

comparing data on ~~the external bus line and data to be output on the~~ each group of the internal bus lines to data on corresponding groups of external bus lines;

when the number of changed bits in a particular group exceeds half of the total number of bits in that group, on the basis of a comparison result, inverting the data on the particular group of internal bus lines to output the data onto the corresponding group of external bus lines; and

outputting a data inversion signal representing that the data in the particular group has been inverted.

9. (Original): A method according to claim 8, wherein the comparison step comprises the step of receiving a clock signal.

10. (Original): A method according to claim 8, further comprising the step of reading out the data on the internal bus line from storage means.

11. (Canceled)